Setting the CH7308 EMI Reduction SSC Value in the VBT

1. Introduction

EMI emissions from the CH7308 can be reduced by lowering the SSC value in the VBT. The VBT or Video BIOS Table is a table located within the VBIOS. To modify the VBIOS, a utility provided by Intel called "Intel BMP" is needed. This application note discuses how to utilize the BMP utility to reduce the EMI emissions of the CH7308. General LVDS settings in the BMP utility are also discussed.

2. Intel BMP Utility

2.1 Loading and editing VBIOS

Using the "Intel BMP" program, load the latest binary VBIOS file (*.dat) and the associated *.bsf file from the Intel ARMS website. To load the VBIOS, chose “open” in the filemenu of the Intel BMP utility then select the file you wish to load. After loading the VBIOS with this utility, you will be able to customize the VBIOS by modifying various BIOS field parameters. When a field parameter is modified, an asterisk will appear to the left of the corresponding field description. This indicates that the binary .dat file has not been saved yet. After all the LVDS settings has been modified to accommodate the specific system specifications, save the *.dat file and integrate it into the system BIOS.

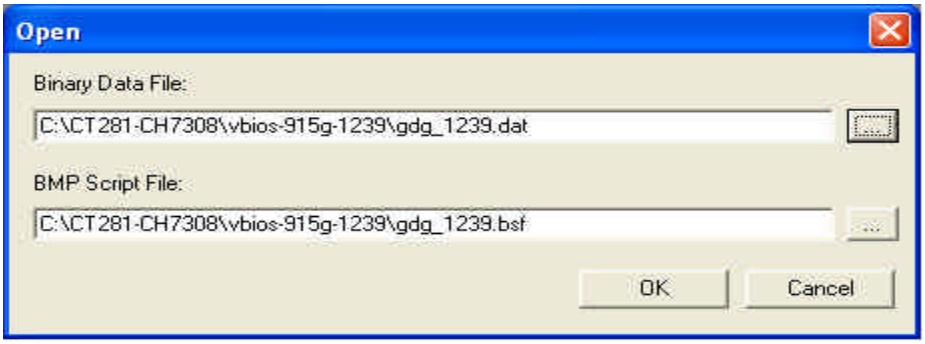

Figure 1: Loading and Opening the binary VBIOS file

2.2 General Information regarding the BMP utility

2.2.1 System BIOS Hooks

Hooks are flags that indicate that the BMP settings are to be overridden. When hooks are enabled then the related CMOS BIOS settings will take into effect. There are 3 types of BIOS Hooks; (5F34h) Set Panel Fitting Hook, (5F35h) Boot Up Display Device Hooks, and (5F40h) Panel Type Hooks. Hooks are enabled by selecting "Use Interrupt 15h" in the pull-down menu in the BMP utility. See Figure 2.

In the case of Panel Type Hooks, if this feature is disabled, the perferred panel timings selected in the General SDVO-LVDS Features will be used regardless of which “panel type” the user selects in the CMOS BIOS page. See Figure 4.

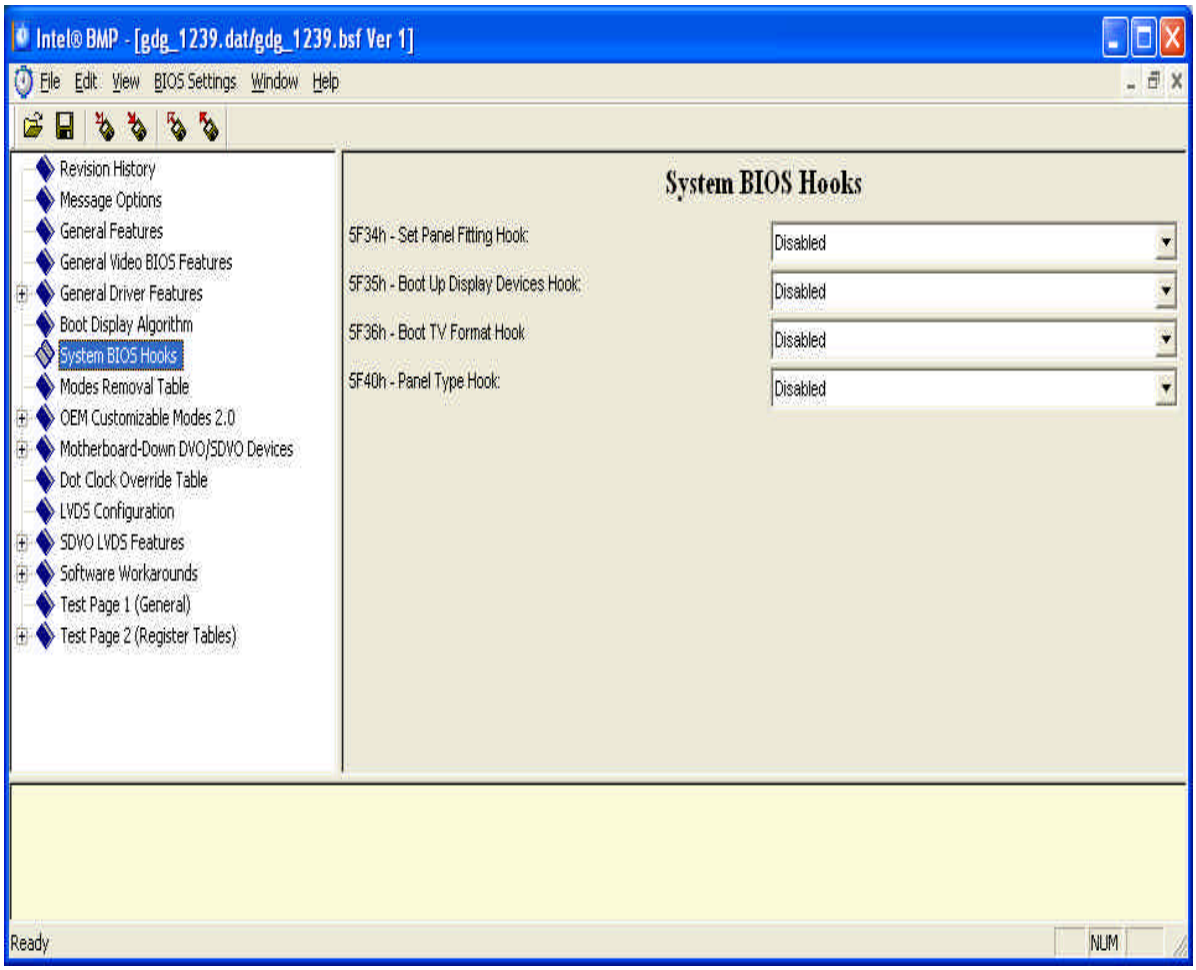

Figure 2: System BIOS Hooks

2.2.2 Motherboard-Down Options

For a CH7308 motherboard-down design, there are features in the VBIOS that must be changed to notify the system that the CH7308 has been implemented this way. In motherboard-down designs, an external ADD2 EEPROM is not needed. The information that is stored in the ADD2 EEPROM of ADD2 card designs is instead stored in the VBT. See Figure 3.

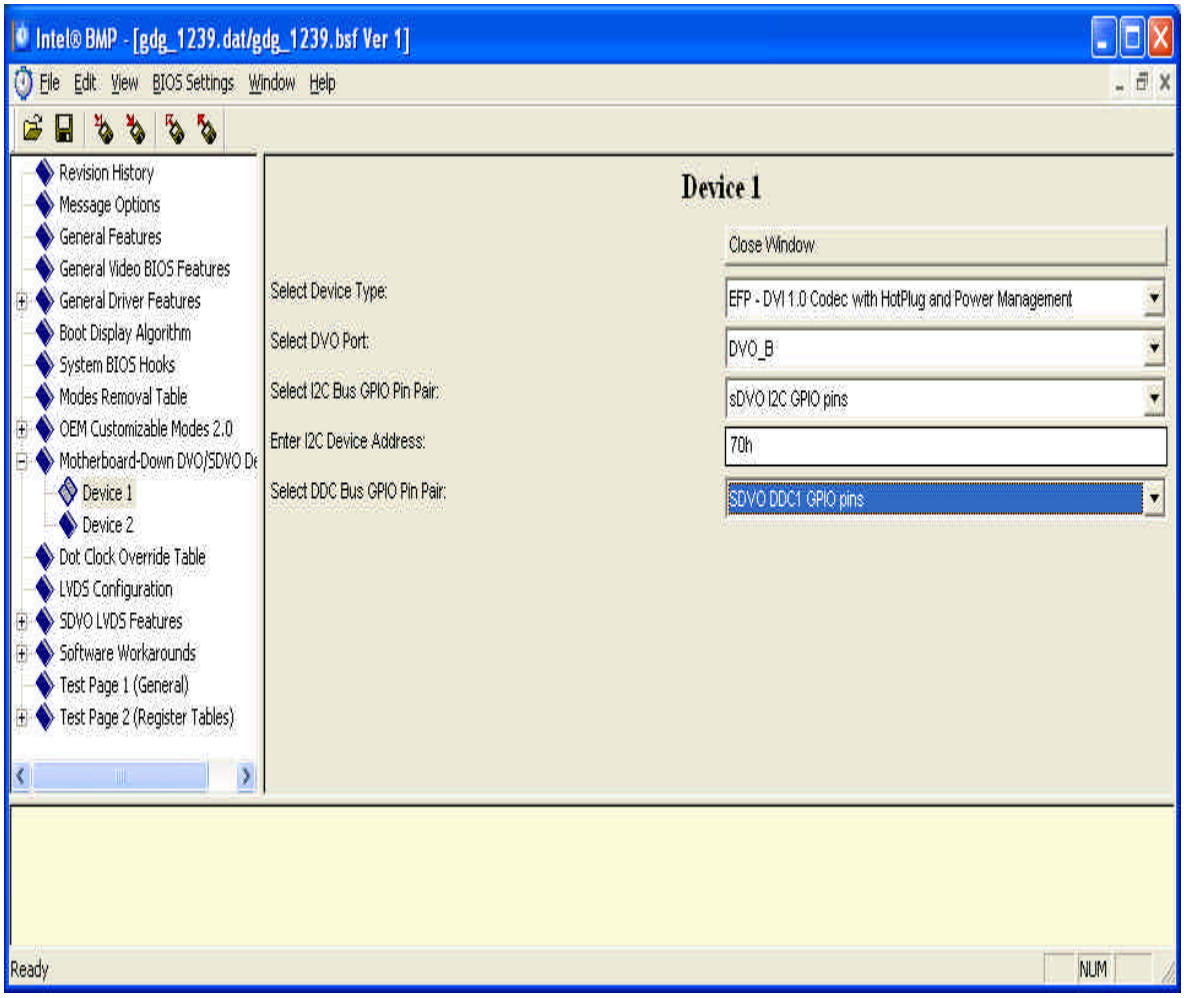

Figure 3: Motherboard down

2.2.3 LVDS Configuration

In the LVDS configuration section there are several LVDS related settings that can be adjusted here. Settings such as panel scaling, up scalar coefficients, dithering, LVDS Channel (single/dual), LVDS SSC support, and LVDS spread spectrum clock frequency.

2.3 EMI Reduction

The CH7308 is capable of lowering the Electromagnetic Interference (EMI) being emitted. To lower the EMI emissions, two fields in the BMP utility must be changed, the "LVDS SSC Support" field and the "LVDS Spread Spectrum Clock Frequency" field. The "LVDS SSC Support" field must first be set to "Enabled." After this field has been changed, the "LVDS Spread Spectrum Clock Frequency" field should be set to a value between 0 to 15. If the “LVDS SSC Support” field is set to "disabled," then the SSC value will be defaulted to "0".

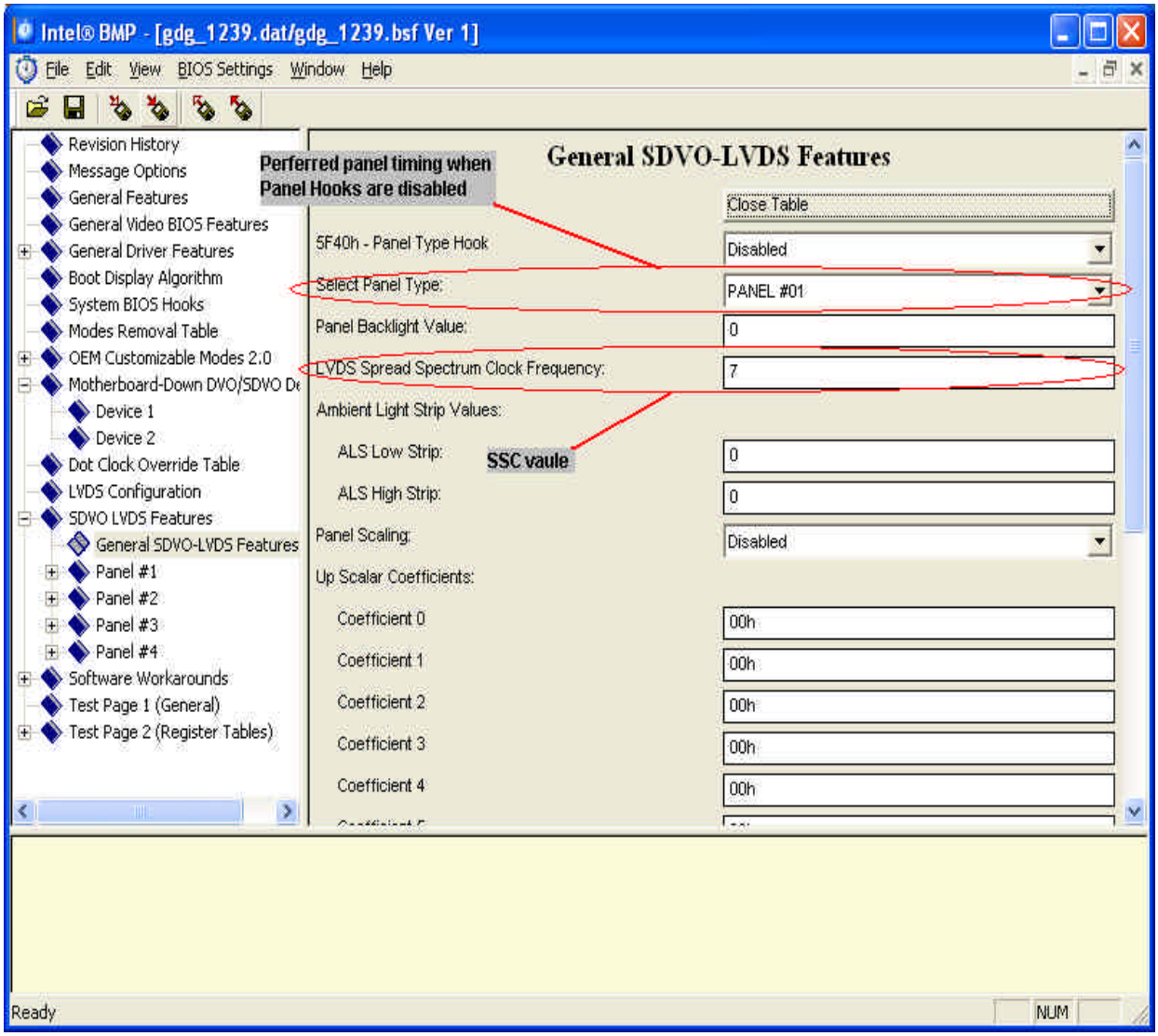

Figure 4: General SDVO BMP Configuration 1

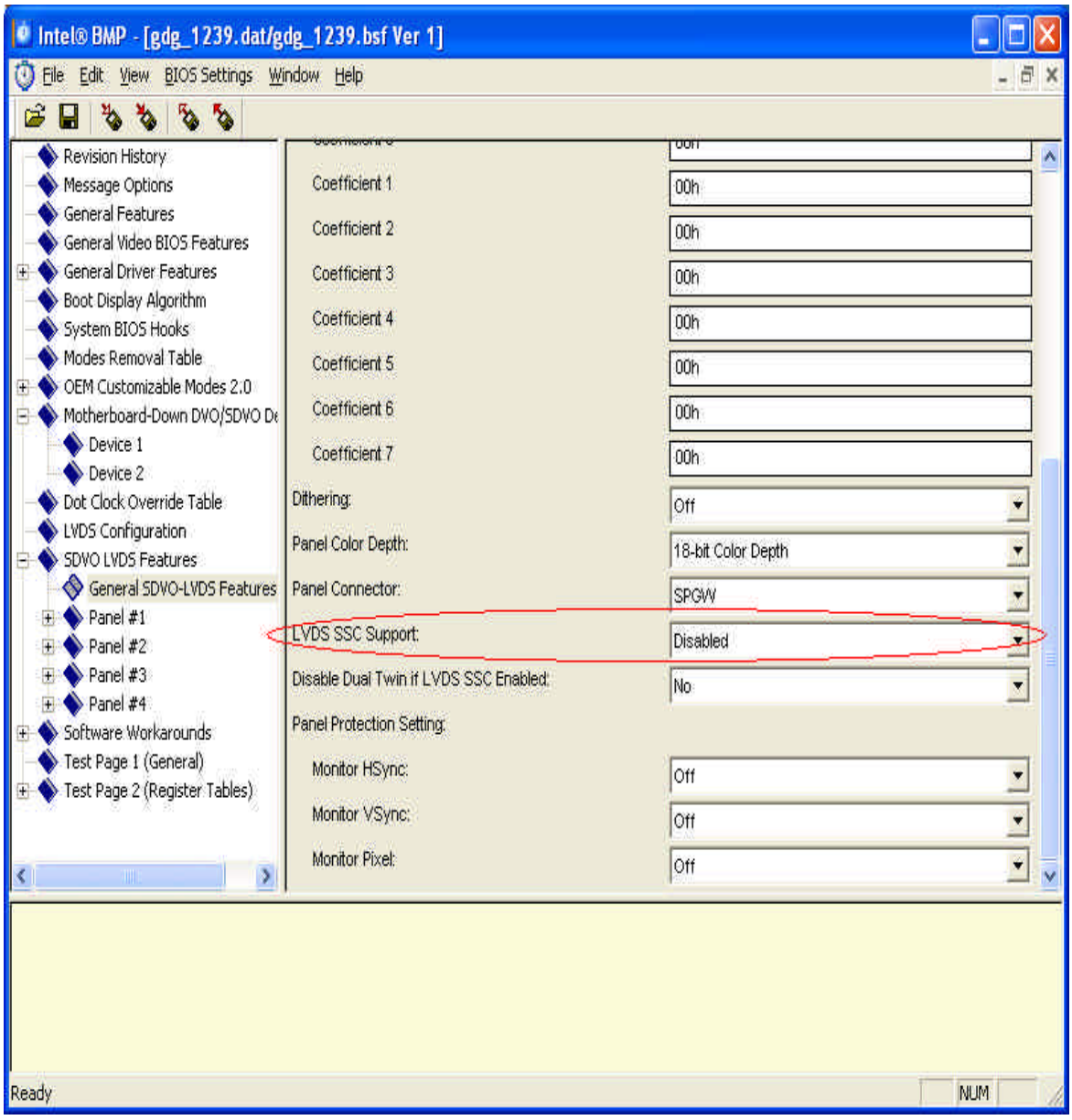

Figure 5: General SDVO BMP Configuration 2

2.4 CH7308A Rev. C vs. CH7308A Rev. D

The EMI reduction circuitry differs between Rev.C and Rev.D of the CH7308A. The differences pertain only to dual channel LVDS panel designs. Designs with single channel LVDS panels are not affected by this change. Below are EMI Reduction vs. SSC value tables of popular LVDS size panels currently available. The SSC values in Table 1 and Table 2 refers to the binary equivalent value entered in the "LVDS Spread Spectrum Clock Frequency" field. Fc is the center frequency of the LVDS panel. For dual channel LVDS panels the center frequency is the maximum pixel rate divided by 2. The CH7308A Rev.D provides more flexibility when changing SSC value the % of total spreading on a dual channel LVDS panel. When migrating from the CH7308A Rev. C to the CH7308A Rev. D for dual LVDS panel designs, careful attention should be made when selecting an SSC value.

CH7308A Rev C % of total spreading						
SSC Value	**800x600 OpenLDI 18bit single channel**	**1024x768 OpenLDI 18bit single channel**	**1280x1024 OpenLDI 18bit single channel**	**1280x1024 SPWG 24bit dual channel**	**1400x1050 OpenLDI 18bit dual channel**	**1600x1200 OpenLDI 18bit dual channel**
0000	0.08	0.05	0.03	0.09	0.06	0.04
0001	0.09	0.06	0.03	1.47	1.47	0.04
0010	0.09	0.65	0.51	2.91	2.92	0.41
0011	0.09	1.24	0.99	4.57	4.58	0.78
0100	0.09	1.84	1.46	6.22	6.24	1.15
0101	1.58	2.43	1.93	7.67	7.71	1.69
0110	1.60	3.01	2.40	9.34	9.36	2.23
0111	1.60	3.60	2.89	10.73	10.75	2.43
1000	1.60	4.18	3.35	12.19	12.39	2.80
1001	1.60	4.76	3.83	13.82	13.85	3.16
1010	1.60	5.08	4.30	15.47	15.49	3.36
1011	3.08	5.39	4.53	16.77	16.93	3.73
1100	3.10	5.96	4.78	18.38	18.42	4.10
1101	3.12	6.27	5.23	19.66	20.12	4.46
1110	3.12	6.57	5.29	21.49	21.59	4.83
1111	3.12	7.16	5.66	22.98	22.98	5.19
Fc:	**40000**	**65000**	**108000**	**54000**	**54000**	**81000**

Figure 6: CH7308A Rev C % of total spreading

CH7308A Rev D % of total spreading						
SSC Value	**800x600 OpenLDI 18bit single channel**	**1024x768 OpenLDI 18bit single channel**	**1280x1024 OpenLDI 18bit single channel**	**1280x1024 SPWG 24bit dual channel**	**1400x1050 OpenLDI 18bit dual channel**	**1600x1200 * OpenLDI 18bit dual channel**
0000	0.08	0.05	0.03	0.06	0.06	N/A
0001	0.08	0.09	0.03	0.06	0.06	N/A
0010	0.08	0.70	0.54	0.53	0.54	N/A
0011	0.08	1.32	1.02	0.98	0.99	N/A
0100	0.08	1.72	1.48	1.23	1.22	N/A
0101	1.60	2.46	1.94	1.59	1.49	N/A
0110	1.60	2.77	2.47	1.96	1.96	N/A
0111	1.60	3.58	2.69	2.43	2.43	N/A
1000	1.60	4.26	3.40	2.89	2.87	N/A
1001	1.60	4.46	3.70	3.11	3.35	N/A
1010	1.60	4.92	3.89	3.39	3.39	N/A
1011	3.05	5.38	4.35	3.85	3.83	N/A
1100	3.10	6.00	4.75	4.31	4.31	N/A
1101	3.13	6.31	5.00	4.56	4.33	N/A
1110	3.13	6.54	5.28	4.81	4.81	N/A
1111	3.13	7.08	5.56	5.28	5.28	N/A
Fc:	**40000**	**65000**	**108000**	**54000**	**54000**	**81000**

***** The CH7308A maximum pixel rate is 140MP/s, 1600x1200 is not valid resolution.

Figure 7: CH7308A Rev D % of total spreading

3. Revision History

Revision	Date	Section	Description
1.0	10/17/05	All	First Revision.
1.1	2/7/06	All	Changed CH7308A to CH7308 where information relates to both the CH7308A and CH7308B

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