CH7513A DP/eDP to LVDS or DP/eDP Converter

FEATURES

- Supports DisplayPort (DP) Specification version 1.3 and Embedded DisplayPort (eDP) Specification version 1.4.
- Support 2 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s link rate
- Supports input color depth 6, 8-bit per pixel in RGB format
- Supports Enhanced Framing Mode
- Support VESA and CEA timing standards up to 1920x1200 resolution in 8-bit input with 60Hz refresh rate
- Support dynamic refresh rate switching
- Fast and full Link Training for embedded DisplayPort system
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- 2 Lane DP/eDP bypass supported with high speed buffer/switch integrated, pass through AUX CH/HPD in eDP / DP bypass application
- 2 work modes: connect 27MHz crystal, inject 27MHz clock
- De-SSC supported
- High-speed Mux integrated to support DP/eDP output pin-multiplexed with LVDS output
- Programmable LCD panel power sequence
- Support 18-bit Single Port, 18-bit Dual Port, 24-bit Single Port and 24-bit Dual Port LVDS output interface
- Support both OpenLDI and SPWG bit mapping for LVDS application
- Support panel select by GPIO pins control or writing the chip registers.
- Support flexible LVDS output pin swapping for top or bottom mount PCBs
- Support internal test pattern
- Blank panel during invalid input
- Supports PWM Backlight luminance level control through AUX channel, PWM pin and BLUP/BLDN pin
- Support Dynamic Backlight Control
- Hot Plug Detection
- Aux switch integrated
- Loads Boot ROM automatically upon power up
- Serial BOOT ROM data updated through I2C bus or AUX Channel
- Support power management mechanism through AUX
- Offered in a 68-pin QFN package

GENERAL DESCRIPTION

Chrontel's CH7513A is a low-cost, low-power semiconductor device that translates the Embedded DisplayPort signal to the LVDS **(**Low-voltage Differential Signaling). This innovative DisplayPort receiver with an integrated LVDS transmitter is specially designed to target the All-In-One PC and the notebook market segments. Through the CH7513A's advanced decoding / encoding algorithm, the input DP/eDP high-speed serialized video data can be seamlessly converted to LVDS, a popular display technology for high-speed serial links in mid/large-sized LCD displays. Leveraging the DP/eDP's unique source/sink "Link Training" routine, the CH7513A is capable of instantly bring up the video display to the LCD when the initialization process is completed between CH7513A and the graphic chip.

The CH7513A is designed to meet the DisplayPort (DP) Specification version 1.3 and the Embedded DisplayPort Specification version 1.4. In the device's receiver block, which supports two DP/eDP Main Link Lanes input with data rate running at either 1.62Gb/s or 2.7Gb/s, can accept RGB digital formats in either 18-bit 6:6:6 or 24-bit 8:8:8 for LVDS output up to 1920x1200. To comply with GPU's new power saving scheme such as display frame rate reduction, the CH7513A is equipped with the Dynamic Refresh Rate switching method, which can automatically reduce to the low refresh rate supported by the LVDS panel.

The integrated LVDS transmitter supports the single port and the dual ports LVDS outputs to drive display resolution up to WUXGA (1920x1200). CH7513A supports panel select by GPIO[0:3] pins control or writing the chip registers. To reduce EMI emission, the CH7513A's LVDS encoder block has incorporated Spread Spectrum control and its spread percentage can be adjusted through the internal registers.

The Backlight On/Off and the PWM are two luminance control functions designed in the CH7513A LVDS power control module. The brightness control commands sent through AUX Channel can be dynamically translated by CH7513A and converted into LCD backlight control signal. The CH7513A will save the last setting of brightness level into the BOOT ROM and restore it upon power up. The CH7513A can dynamically adjust backlight brigntness according to video stream to save power consumption and it supports OSD display in this way.

The CH7513A will immediately convert the DP/eDP signal to LVDS output after DP/eDP Link Training is completed. This feature can be achieved by loading the panel's EDID and the CH7513A's configuration settings in the serial BOOT ROM connected to the CH7513A. During system power-up and upon completion of the DP/eDP Link Training through AUX Channel, CH7513A will generate LVDS signal according to the panel power-up timing sequencing stored in the BOOT ROM.

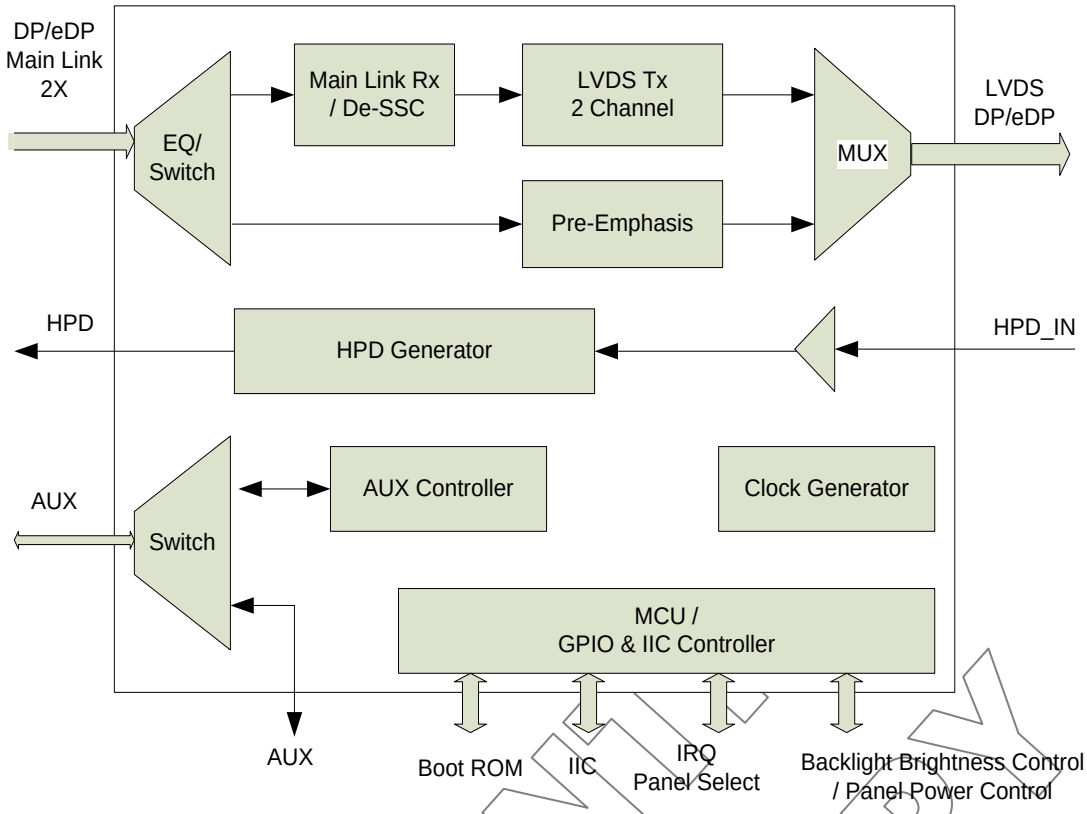

Figure 1: CH7513A Function Block Diagram

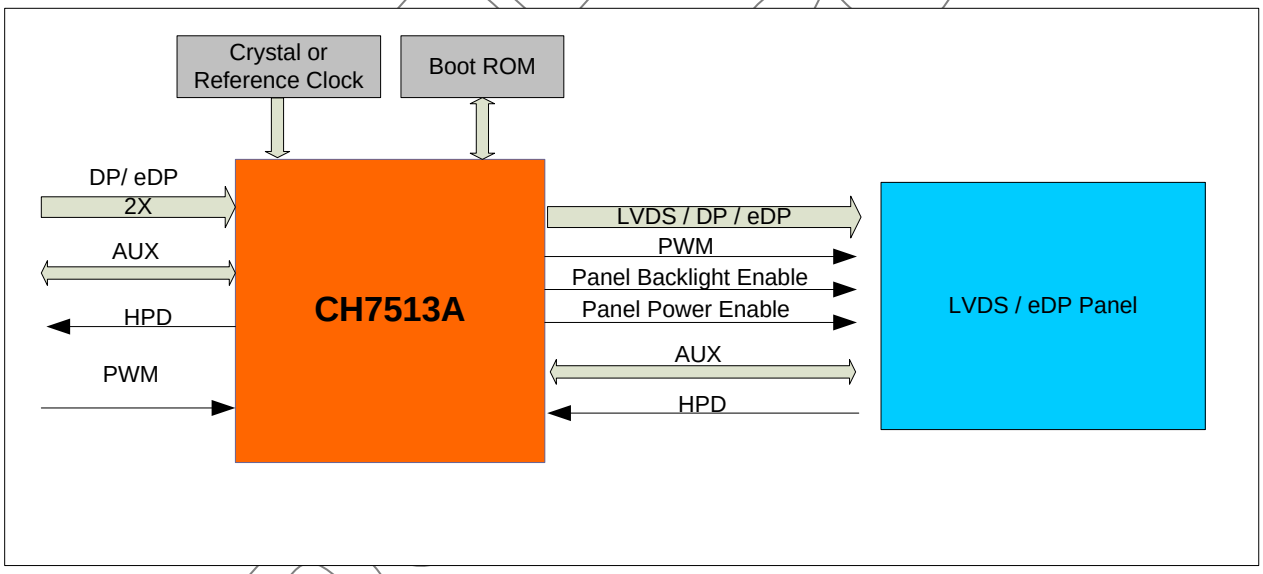

Figure 2: CH7513A Application Diagram

1.0 PIN ASSIGNMENT

1.1 Package Diagram

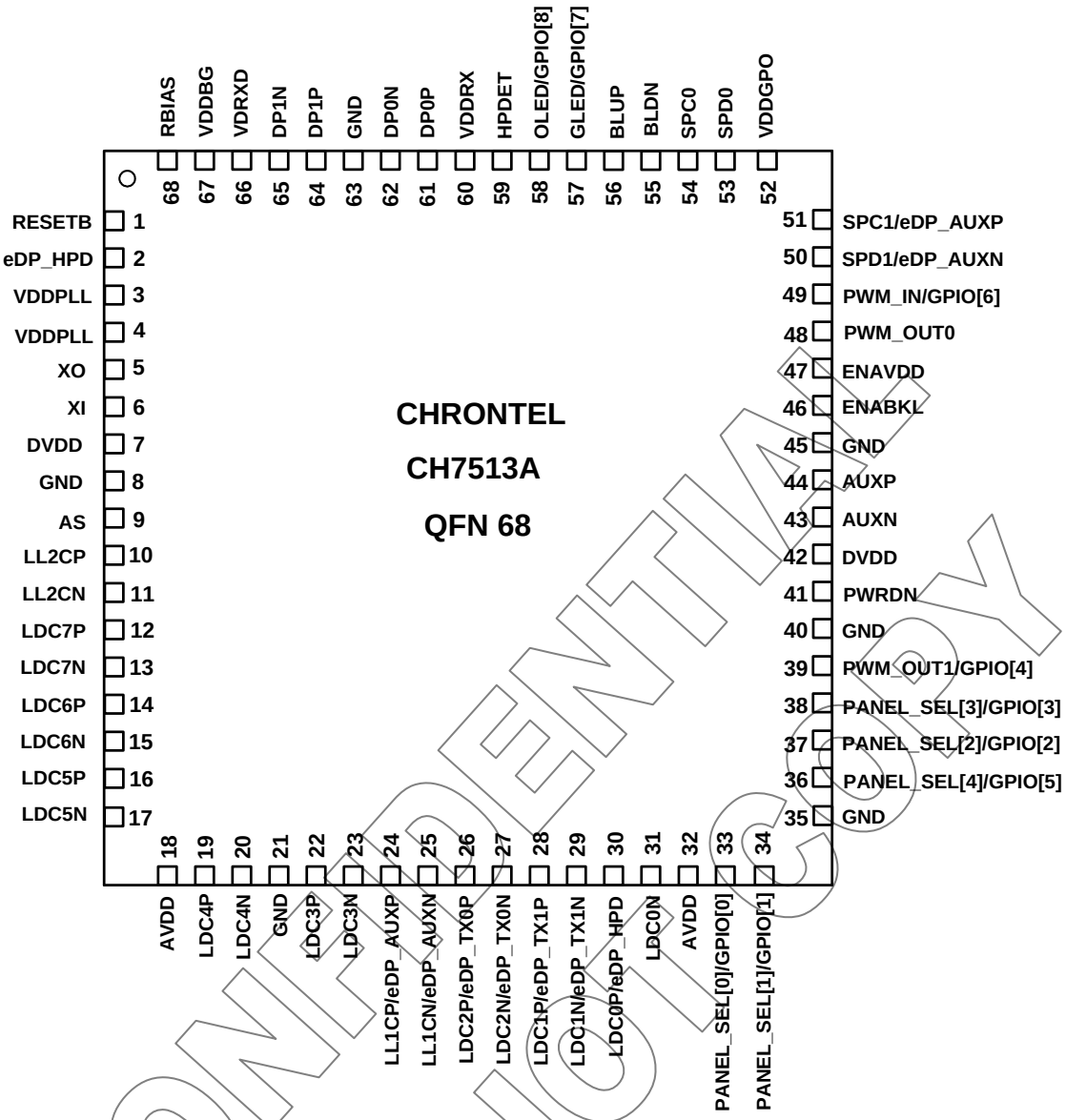

Figure 3: CH7513A 68-pin QFN pin out

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1	In	RESETB	**Reset Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register. It should be pulled high to DVDD with a 10 KΩ resistor.
2	In	eDP_HPD	**eDP Panel / DP HPD Input** Pin 2 and 30 shall not be used at the same time.
5	Out	XO	**Crystal Output** A parallel resonant 27MHz crystal (±20 ppm) should be attached between this pin and XI. Note: 50ppm to pin XO
6	In	XI	**Crystal Input** A parallel resonant 27MHz crystal (±20 ppm) should be attached between this pin and XO. Note: 50ppm to pin XI
9	In	AS	**I2C Slave Device Address Selection**
10~17, 19,20,	Out	LL2CP/N, LDC[7:4]P/N	**LVDS Left Channel Output**
22~31	Out	LL1CP/N, LDC[3:0]P/N	**LVDS Right Channel Output**
	Out	eDP_AUXP/N, eDP_TX[1:0]P/N, eDP_HPD	**eDP/ DP Bypass Ouput**
33~34, 36~38	In	PANEL_SEL[4:0]	**Panel Select Control Signals** These pins could be pulled high (10 KΩ resistor to +3.3V) or low forming into 32 different combinations. Every combination can match with one panel type.
	In/Out	GPIO [3:0],GPIO[5]	**General Input and Output Pins**
39	Out	PWM_OUT1	**PWM Output for Backlight Brightness Dimming** PWM Duty Cycle Range: 30~100%(16 steps) The output Frequency from PWM_OUT1 can be up to 400KHz. Voltage level is 3.3V.
	In/Out	GPIO[4]	**General Input and Output Pin**
41	In	PWRDN	**Power Down Control** CH7513A enters/exit power down state when receiving active low pulse (0V) from this pin.
43,44	In/Out	AUXP, AUXN	**AUX Channel Differential Input/Output** These two pins are eDP/DP AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
46	Out	ENABKL	**LCD Panel Backlight Enable** Enable backlight of LCD panel (3.3V)
47	Out	ENAVDD	**LCD Panel Power Supply Enable** Enable LCD panel VDD (3.3V)
48	Out	PWM_OUT0	**PWM Output for Backlight Brightness Dimming / Bypass PWM_IN** PWM Duty Cycle Range: 0~100%(16 steps) The output Frequency from PWM_OUT0 can be up to 400KHz. Voltage level is 3.3V. Bypass PWM input, and while in bypass mode, frequency of PWM_OUT0 can be up to 1MHz.
49	In	PWM_IN	**Backlight brightness PWM input** PWM_IN has two work modes: Bypass mode and Duty Cycle Multiplication

Pin #	Type	Symbol	Description
			with AUX CH mode. In bypass mode, the input frequency to PWM_IN can be up to 1MHz. In Duty Cycle Multiplication with AUX CH mode, the input frequency to PWM_IN can be up to 50KHz. Voltage level is 3.3V.
	In/Out	GPIO[6]	**General Input and Output Pin**
50	In/Out	SPD1	**Serial Port Data Input/Output for Chip BOOT ROM/EDID** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4KΩ - 9 KΩ pull up resistor to 3.3V.
	In/Out	eDP_AUXN	**AUX Channel Negative Pin** eDP_AUXN and eDP_AUXP pins are eDP / DP AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
51	Out	SPC1	**Serial Port Clock Output for Chip BOOT ROM/EDID** This pin functions as the clock output of the serial port and operates with output from 0 to 3.3V. This pin requires an external 4KΩ - 9KΩ pull up resistor to 3.3V.
	In/Out	eDP_AUXP	**AUX Channel Differential Input/Output** eDP_AUXN and eDP_AUXP pins are eDP AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
53	In/Out	SPD0	**Serial Port Data Input/Output for Register Map** This pin is used to access CH7513A internal registers. It functions as the bi-directional data pin of the serial port and operates with input from 0 to 3.3V. Output is driven from 0 to 3.3V. This pin requires an external 6KΩ - 8 KΩ pull up resistor to 3.3V.
54	In	SPC0	**Serial Port Clock Input for Register Map** This pin is used to access CH7513A internal registers. It functions as the clock input of the serial port and operates with input from 0 to 3.3V. This pin requires an external 6KΩ - 8 KΩ pull up resistor to 3.3V.
55	In	BLDN	**Decrement Backlight Brightness Input**
56	In	BLUP	**Increment Backlight Brightness Input**
57	Out	GLED	**Green LED Control** This pin indicates CH7513A in normal power and mode status. Its output voltage is 3.3V.
	In/Out	GPIO[7]	**General Input and Output Pin**
58	Out	OLED	**Orange LED Control** This pin indicates CH7513A in abnormal power and mode status. Its output flickers from 0 or 3.3V.
	In/Out	GPIO[8]	**General Input and Output Pin**
59	Out	HPDET	**Hot Plug Detect** This output pin is used as the connection detection by a DisplayPort Source system. It generates interrupt pulse as defined by DisplayPort standard. The output voltage is 3.3V. A 100 kΩ resistor should be connected between this pin and GND. It should be linked to DisplayPort source.
61,62 64,65	In	DP[1:0]P/N	**Main Link Lane Input** These pins accept two AC-coupled differential pairs signals from the eDP/DP transmitter.
68	In	RBIAS	**Band-gap Bias input** A 1 KΩ(1%) resistor should be connected between this pin and GND.
3,4	Power	VDDPLL	**Stream PLL Power Supply (1.2V)**

Pin #	Type	Symbol	Description
7,42	Power	DVDD	**Digital Power Supply (1.2V)**
8, 21,35,40, 45, 63	Power	GND	**Power Ground**
18,32	Power	AVDD	**LVDS Driver Power Supply and GPO Power Supply (3.3V)**
52	Power	VDDGPO	**GPIO Power Supply (3.3V)**
60,66	Power	VDDRX	**DP Rx Power Supply (1.2V)**
67	Power	VDDBG	**Band-gap Power Supply (1.2V)**
Thermal Exposed Pad	Power	GND	**Ground**

2.0 PACKAGE DIMENSIONS

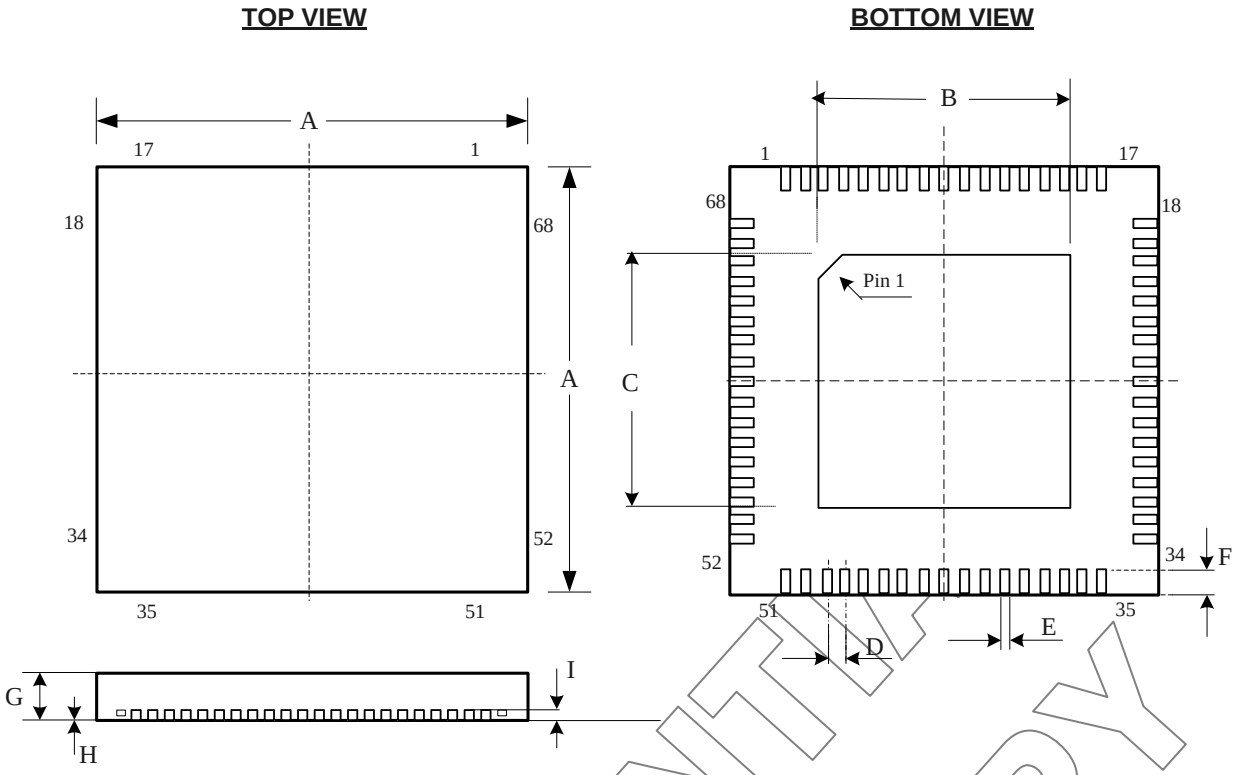

Figure 4: 68 Pin QFN Package (8x8 mm)

Table of Dimensions

No. of Leads		SYMBOL								
68 (8x8 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	7.90	4.30	4.30	0.40 BSC	0.15	0.30	0.70	0	0.203 REF
	MAX	8.10	4.50	4.50		0.25	0.50	0.80	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207

Disclaimer

This document provides technical information for the user. Chrontel reserves the right to make changes at any time without notice to improve and supply the best possible product and is not responsible and does not assume any liability for misapplication or use outside the limits specified in this document. CHRONTEL warrants each part to be free from defects in material and workmanship for a period of one (1) year from date of shipment. Chrontel assumes no liability for errors contained within this document. The customer should make sure that they have the most recent data sheet version. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Chrontel, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Chrontel PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF Chrontel. Life support systems are those intended to support or sustain life and whose failure to perform when used as directed can reasonably expect to result in personal injury or death.

ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7513A-BF	68QFN, Lead-free	Commercial : 0 to 70°C	260/TRAY
CH7513A-BFI	68QFN, Lead-free	Industrial : -40 to 85°C	260/TRAY

Chrontel

www.chrontel.com

E-mail: sales@chrontel.com